REMARKS

Reconsideration is requested.

An election between Species 1 and Species 2 is being required. An election was previously made in applicant's response filed January 22, 2003, in which. More particularly, Species 1 was elected for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Claims 50-60 were previously canceled.

Claims 11-15 stand rejected under 35 U.S.C. §101 double patenting as being unpatentable over claims 18-36 of U.S. Patent Application No. 09/388,856. U.S. Patent Application No. 09/388,856 is now U.S. Patent No., 6,579,751.

A "same invention" double patenting rejection requires identical subject matter. According to the MPEP, the test is whether there is an embodiment of the invention that falls within the scope of one claim, but not the other. If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist.

The double patenting rejection is not proper for multiple reasons.

First, Claim 11 of the present application recites "devices" while claims 18-36 of application Serial No. 09/388,856 specify n-type transistor devices.

Second, claims 18-36 of application Serial No. 09/388,856 recite forming transistor devices having source regions and drain regions, while claim 11 of the present application does not.

Third, claims 12-15 of the present application variously recite "field effect transistors" while none of claims 18-36 of the prior application specifically recite "field effect" transistors.

Therefore, claims 11-15 are of different scope than claims 18-36 of the prior application. Therefore, the "same invention" type double patenting rejection is improper and should be withdrawn.

Claims 5-10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,534,449 to Dennison et al.

Anticipation under 35 U.S.C. §102 is a standard of strict identity. The factual determination of anticipation requires the disclosure in a single reference of every element of the claimed invention. *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). "It is axiomatic that for prior art to anticipate under * 102 it has to meet every element of the claimed invention...." *Hybritech Inc. v. Mononclonal Antibodies, Inc.*, 802 F.2d 1367, 234 USPQ 81, 90 (Fed. Cir. 1986). "It is elementary that an anticipation rejection requires a showing that each limitation of a claim must be found in a single reference, practice, or device." *In re Donohue*, 766 F.2d 531, 226 USPQ 619, 621 (Fed. Cir. 1985).

Claim 5 recites a semiconductor processing method comprising a masking step providing a common mask; and an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

The Dennison et al. reference fails to teach or suggest conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, in combination with the other features of claim 5. Instead, the method disclosed in the Dennison et al. '449 reference would result in devices having two different threshold voltages. More particularly, Fig. 2 of the Dennison et al. reference shows areas 26 and 22 that are completely masked by masking layer (38) and area 18 that is not masked. The areas 26 and 22 are both similarly masked and would not result in devices having different threshold voltages.

Further, for a proper rejection under 35 U.S.C. §102, it is incumbent upon the Examiner to identify where each and every facet of the claimed invention is disclosed in the applied reference. *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick*, 730 F.2d 1452, 221 USPQ 481 (Fed. Cir. 1984). If the examiner maintains that the rejection is proper, the examiner is requested to identify where the Dennison et al. reference teaches conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages. It is respectfully suggested that the examiner will not be able to do so.

Therefore, claim 5 is allowable.

As claims 6-15 depend on claim 5, they too are allowable.

In view of the foregoing, allowance of claims 5-15 is respectfully requested.

A telephonic interview is requested in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time.

Respectfully submitted,

Dated: June 30, 2003 By: _____

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Application Serial No. 09/848,846
Filing Date ..... May 3, 2001
Inventor ..... Luan C. Tran
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Laura M. Schillinger
Attorney's Docket No. MI22-1689
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 8, 2003 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

5. A semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

6. The method of claim 5, wherein said three devices comprise peripheral circuitry.

7. The method of claim 5, wherein said three devices comprise NMOS field effect transistors.

8. The method of claim 5, wherein said three devices comprise NMOS field effect transistors comprising peripheral circuitry.

9. The method of claim 5, wherein the three devices comprise PMOS field effect transistors.

10. The method of claim 5, wherein said three devices comprise PMOS field effect transistors comprising peripheral circuitry.

11. The method of claim 5, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices.

12. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

13. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise NMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

14. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors; and

said portions comprise portions of peripheral circuitry devices.

15. The method of claim 5, wherein:

the common masking step comprises masking only portions of some of the devices which receive the halo implant;

said devices which receive the halo implant comprise PMOS field effect transistors having source regions and drain regions; and

said portions comprise portions of peripheral circuitry devices, wherein said masking comprises masking only one of the source region and drain region for one of the three devices, and exposing both of the source region and drain region for another of the three devices.

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